

Sub E1 30

1 ~~180.~~ (amended) An integrated circuit device comprising:  
 2 input receiver circuitry to sample an operation code synchronously  
 3 with respect to a first transition of an external clock signal;  
 4 output driver circuitry to output data in response to the  
 5 operation code specifying a read operation, wherein:  
 6 the output driver circuitry outputs a first portion of data  
 7 in response to a rising edge transition of the external clock  
 8 signal; and  
 9 the output driver circuitry outputs a second portion of data  
 10 in response to a falling edge transition of the external clock  
 11 ~~signal.~~

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1 ~~181.~~ The integrated circuit device of claim ~~180~~ further including  
 2 a memory array having a plurality of memory cells.

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1 ~~182.~~ The integrated circuit device of claim ~~181~~ wherein the input  
 2 receiver circuitry receives address information synchronously with  
 3 respect to the external clock signal.

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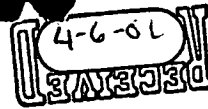
1 ~~183.~~ (amended) The integrated circuit device of claim ~~182~~ wherein  
 2 the input receiver circuitry samples the address information  
 3 synchronously with respect to a second transition of the external clock  
 4 signal.

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1 ~~184.~~ The integrated circuit device of claim ~~183~~ wherein the  
 2 operation code and the address information are included in a packet.

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1 <sup>35</sup>~~185~~. The integrated circuit device of claim <sup>30</sup>~~180~~ further including  
2 a clock alignment circuit to receive the external clock signal.

1 <sup>36</sup>~~186~~. The integrated circuit device of claim <sup>35</sup>~~185~~ wherein the clock  
2 alignment circuit generates an internal clock signal, and the output  
3 driver circuitry outputs data in response to the internal clock signal.

1 <sup>37</sup>~~187~~. (amended) The integrated circuit device of claim <sup>30</sup>~~180~~ wherein  
2 both the rising and falling edge transitions of the external clock  
3 signal include voltage swings of less than one volt.

1 <sup>38</sup>~~188~~. (amended) The integrated circuit device of claim <sup>30</sup>~~180~~ wherein  
2 the rising edge transition of the external clock signal and the falling  
3 edge transition of the external clock signal transpire in one clock  
4 cycle of the external clock signal.

1 <sup>39</sup>~~189~~. The integrated circuit device of claim <sup>30</sup>~~180~~ wherein the input  
2 receiver circuitry receives block size information synchronously with  
3 respect to the external clock signal, wherein the block size  
4 information indicates an amount of data to be output by the output  
5 driver circuitry.

1 <sup>40</sup>~~190~~. (amended) The integrated circuit device of claim <sup>30</sup>~~180~~ wherein  
2 the input receiver circuitry receives a value which is representative  
3 of a number of clock cycles of the external clock signal to transpire  
4 before the output driver circuitry outputs data.

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- 1 ~~191~~. (amended) The integrated circuit device of claim ~~190~~ further
  - 2 including a programmable register to store the value which is
  - 3 representative of a number of clock cycles of the external clock signal
- to transpire before the output driver circuitry outputs data.
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